Attorney Docket: 042390.P8836

APPLICATION FOR UNITED STATES LETTERS OF PATENT

FOR

BUFFER ALLOCATION CIRCUIT

Inventor(s): **BRIAN K. HOLSCHER**

Prepared by:

BLAKELY SOKOLOFF TAYLOR & ZAFMAN, LLP
12400 Wilshire Boulevard, 7th Floor
Los Angeles, California 90025
(425) 827-8600

"Express Mail" Label Number EL 431686995US

Date of Deposit June 30, 2000

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Box Patent Application, Washington, D.C. 20231.

Dominique Valentino 6-30-00
Dominique Valentino Date

Attorney Docket: 042390.P8836
*Express Mail No.*EL______________

MINIMUM GATE COUNT BUFFER ALLOCATION CIRCUIT

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention generally concerns buffer allocation in processing devices, and in particular concerns allocation of a next available buffer in a microprocessor.

2. Background Information

A common approach in trying to find the next available buffer in a processing device is to implement priority encoders, which determine the next available buffer through use of a pointer to the current buffer and a bit vector representing the combination of available buffers. For each pointer position, a priority encoder determines the next buffer from the available buffer bit vector. For example, if 8 buffers were to be implemented in this manner, 8 priority encoders would typically be used. The output of all the encoders is then driven to a multiplexer (mux), which uses the pointer to the current buffer to pick which encoder's output to use. Each encoder is for a different pointer value, and accordingly, cannot be shared by other pointer values.

The following truth tables correspond to an exemplary 3-buffer configuration that employs priority encoders.

Encoder 0:

Input	Output
000	000
001	001
010	010

011	010
100	100
101	100
110	010
111	010

Encoder 1:

Input	Output
000	000
001	001
010	010
011	001
100	100
101	100
110	100
111	100

Encoder 2:

Input	Output
000	000
001	001
010	010
011	001
100	100
101	001
110	010
111	001

Output Mux
(Input is current pointer and guaranteed to have one and only one bit set):

Input	Output
001	Encoder0
010	Encoder1
100	Encoder2

As the number of buffers increase, the number of input and output bits for each encoder also increases. Furthermore, this requires an increase in the size of the mux, as well. As a result, there is an almost exponential growth in the required logic as the number of buffers increase. Accordingly, an improved approach is desired.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing aspects and many of the attendant advantages of this invention will become more readily appreciated as the same becomes better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

FIGURE 1 is a block diagram illustrating the inputs and outputs of a computational cell implemented by the present invention;

FIGURE 2 is a block schematic diagram illustrating a cascaded array of computational cells in accord with an exemplary embodiment of the invention;

FIGURE 3 is a detailed schematic diagram illustrating a set of logic gates employed in a exemplary embodiment of the computational cell;

FIGURE 4 is a block schematic diagram in accord with FIGURE 2 illustrating the logic values at each of the inputs and outputs of the logic circuits in the array of computational cells under a predefined starting condition; and

FIGURE 5 is a block schematic diagram of a processor that includes an array of buffers that are allocated through use of the array of computational cells an accord with the present invention.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

The present invention comprises circuitry that enables selection of the next available entry in an array of buffers based on an available vector and a current selected entry vector. In general, buffers within an array of some quantity of buffers are desired to be accessed by devices such as microprocessors for temporary storage of data. The actual quantity of buffers that may be accessed through implementation of the present invention, as described below, is not limited. For convenience, the quantity of buffers will be denoted as *b* buffers, since the invention is extendible to any value of b > 1 buffers.

In one embodiment, the circuitry comprises a quantity of computational cells that are organized such that there is a one-to-one correspondence to respective buffers among the quantity of buffers that are desired to be accessed (i.e., the quantity of computational cells is equal to the quantify of buffers (= *b*)). With reference to FIGURES 1-4, each computational cell is denoted by *Cx*, wherein x is in the range of 0 to *b*-1. As shown in FIGURE 1, each computational cell *Cx* has 3 inputs, denoted *Ax*, *Px*, and *Ix*, and two outputs, denoted *0x* and *Nx*, and includes combinational logic to calculate each of the 2 outputs and 3 inputs. FIGURE 2 illustrates an exemplary buffer allocation circuit 10 comprising an array of 8 computational cells Cx coupled together in a cascaded fashion, wherein each computation cell receives input data and provides output data corresponding to a respective buffer Bx (i.e., B[0], B[1], etc.), in a buffer array 12.

The inputs *Ax*, *Px*, and *Ix* to the array of computational cells are defined as follows. The *Ax* inputs collectively define an availability vector consisting of 1 bit for each buffer (i.e., 1 bit for each computational cell *Cx*). Each bit is asserted (i.e., 1) when a buffer is available for use and de-asserted (i.e., 0) if the buffer is being used. Each bit of the availability vector is connected to a corresponding *Ax* input. The *Px*

inputs collectively define a current selected entry vector consisting of 1 bit for each buffer. One bit is asserted at a time in the selected entry vector, indicating which entry or buffer was the last to be selected. Each bit of this selected entry vector is connected to a corresponding *Px* input. As shown in FIGURE 2, The *Ix* inputs are connected to a respective *Ox* output from a preceding (i.e., adjacent) cell. For example, the I(1) input is connected to the O(0) output, the I(2) input is connected to the O(1) output, etc. In addition, the I(0) input is connected to the O(*b*-1) output.

Outputs *Ox* and *Nx* from the array of computational cells are as follows. The *Nx* outputs form a next availability vector consisting of 1 bit from each computational cell, wherein each bit is connected to a corresponding *Nx* output. Only 1 bit is asserted at any one time, wherein the asserted bit represents the next selected entry. The *Ox* outputs are connected to the *Ix* inputs of the next cell (i.e., the cell to the immediate left), and comprise logic values based on the equations defined below.

Each computational cell *Cx* includes logic to implement the following logic equations:

$$N = A \text{ AND } I \qquad (1)$$

$$O = P \text{ OR } (\text{NOT } A \text{ AND } I) \qquad (2)$$

An exemplary logic circuit 14 for implementing the foregoing logic equations is shown in FIGURE 3, and includes a pair of AND gates 16 and 18, an inverter 20, and an OR gate 22. AND gate 16 produces an *Nx* output by logically ANDING *Ax* and *Ix* inputs. AND gate 18 produces an output 24 by logically ANDING the *Ix* input and an inverted *Ax* input, which is inverted by inverter 20. Output 24 of AND gate 18 is then logically OR'ed with input *Px* (by OR gate 22) to produce output *Ox*. As will be recognized by those skilled in the art, other logic circuit components may be implemented to produce similar outputs in accord with equations (1) and (2).

With reference to FIGURE 4, an exemplary data configuration corresponding to a current usage of buffers B[0] – B[7] in buffer array 12 is illustrated, wherein buffers B[0] and B[1] are in current use, and buffer B[1] is the current selected buffer. Accordingly, the *Ax* data is defined by an available vector 26 with a value of [11111100], indicating that buffers B[0] and B[1] are currently in use, while buffers B[2] – B[7] are available. Furthermore, the *Px* data collectively comprises a current selected entry vector 28 with a value of [00000010], indicating that buffer B[1] is the currently selected buffer, and the *Nx* data collectively comprise a next available vector 30 with a value of [00000100], indicating that the next available buffer is B[2]. Once buffer B[2] is allocated for use, the value of available vector 26 will change to [11111000], the value of selected entry vector 28 will change to [00000100], and the value of next available vector 30 will change to [00001000], indicating the buffer B[3] is the next available buffer.

The present invention may be implemented in various logic devices, such as a processor 32 shown in FIGURE 5. Processor 32 includes a buffer allocation circuit 34 that is substantially similar to buffer allocation circuit 10, which is used to allocate buffers from among an array of buffers 36. In addition, processor 32 includes typically processing circuitry, such as functional units, cache, etc., (all not shown).

The above description of illustrated embodiments of the invention is not intended to be exhaustive or to limit the invention to the precise forms disclosed. While specific embodiments of, and examples for, the invention are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize.

Although the present invention has been described in connection with a preferred form of practicing it and modifications thereto, those of ordinary skill in the

art will understand that many other modifications can be made to the invention within the scope of the claims that follow. Accordingly, it is not intended that the scope of the invention in any way be limited by the above description, but instead be determined entirely by reference to the claims that follow.